Challenges of developing resonant cavity photon-counting detectors at 1064nm

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ABSTRACT

Deep Space Optical Communications (DSOC)) impose challenging requirements on detector sensitivity and bandwidth [1]. The current state-of-the art of high-repetition rate, high-power lasers recommends using near-infrared (NIR) 1064nm wavelengths for specific DSOC tasks [2]. Large photonic arrays with integrated beam acquisition, tracking and/or communication capabilities, and smart pixel architecture should allow the implementation of more reliable and robust DSOC systems. Integration of smart pixel technology for parallel data read, acquisition and processing is currently available in silicon. Therefore it would be desirable to monolithically integrate the photodetectors with the electronics. However, silicon has a weak absorption at 1064nm. One elegant approach to increase its absorption efficiency is to trap the photons inside the silicon using the cavity resonance effect (resonant cavity enhancement or RCE).

We present in this paper the challenges of developing resonant cavity single-photon detector arrays for applications to DSOC. The metrics of the main process parameters to fabricate resonant cavity detectors is analyzed and critical process steps are developed and evaluated.

We conclude that such detector arrays are feasible using current state-of-the-art CMOS technology, provided that suitable process control protocols are developed. We report a 10X performance enhancement at NIR wavelengths for the first generation of resonant cavity single-photon detector prototypes, less than 150ps timing performance in photon-starved mode and 20-30ps for multi-photon hits.

Keywords: 1064nm, DSOC, Geiger, RCE, single-photon detection.

1. INTRODUCTION

Single-photon detection technology with silicon Geiger avalanche PhotoDiode (GPD) arrays has demonstrated maturity and has been already used in a wide variety of applications (biomedical, defense, nuclear physics and space). The analysis of long-range optical communications designs have concluded that near-infrared (NIR) laser systems are a promising candidate. It would be desirable to capitalize on the progress on GPD technology and explore whether incremental GPD structure design and silicon GPD technology enhancements will yield detector systems suitable for DSOC. Silicon is weakly absorbing photons at 1064 nm, the NIR wavelength of choice for the application. GPD structures with extended electric field and thin absorption thickness could yield high collection efficiency of photo-generated carriers. If weakly absorbed photons could be trapped in the silicon GPD, the intrinsic quantum absorption efficiency would approach 100%. Developments in resonant cavity physics and particularly in resonant cavity silicon detectors indicate that resonant cavity enhancement (RCE) concept could provide a robust solution to increasing the GPD array overall quantum efficiency at 1064 nm. Indeed, the RCE concept, requiring precise cavity tuning and high reflectance mirrors (distributed Bragg reflectors or DBR) seems to be fully compatible with the GPD structure and it

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hints that incremental GPD structure design modifications based on today's state-of-the-art silicon processing tools will allow taking full advantage of the resonant cavity process.

DBR mirrors could be integrated in a CMOS [3], integrated with silicon technology [4] or with Ge/Si technology [5]. Based on the current GPD array designs at aPeak, we anticipate that RC-GPD arrays with integrated avalanche quenching and readout will require processing in 180nm and 130nm technology nodes [6]. DBR integration at the front end of the fabrication process flow requires customized process step modifications which involve high NRE costs and restricts portability to other CMOS foundry. Our approach is to use standard CMOS processing to fabricate the RC-GPD array and implement RCE at the back end of the fabrication process. Because cavity and DBR fabrication allow low-temperature processing, the GPD array doping profiles are not altered/degraded. Thus, it should be feasible to merge standard CMOS technology with custom RCE processing into a robust technology capable of fabricating a new, cost-effective detector with single photon detection performance, design flexibility and suitable for high volume manufacturing.

The quantum efficiency in RC-GPD is enhanced by thinning the GPD to create a resonant cavity that traps the incident photons and may increase their absorption efficiency close to 100% (for loss-free cavities). If the RC-GPD structure is designed to efficiently collect most of the electron-hole pairs generated by the trapped photons, then the quantum efficiency at the resonant wavelength could reach 100%.

As the RC-GPD structure could be now designed thin, the electrical crosstalk between closely spaced GPDs is lowered, thus allowing closely packed RC-GPD arrays. Using RCE in weakly absorbing semiconductors is essential for achieving high spatial resolution photon counting arrays. DBR mirrors fabricated at the cavity boundaries are capable of high, selective reflectance that leads to resonant absorption in semiconductor. Without DBR mirrors, thick GPDs with very wide space charge regions (100 μm – 150 μm) and operated at thousands of volts could collect efficiently the carriers generated by the near infrared photons, but it would require similar spatial separation to avoid severe crosstalk between adjacent pixels. Such operation voltage is not compatible with today's CMOS electronics. Alternatively, the operation voltage for our GPD technology is only 13-15 volts, the space charge region width is in the 5-10 μm range and carriers are collected through diffusion from 20-30 μm. Using RCE is ideal for this GPD design as the carrier collection depth matches well the thickness of the silicon cavity that could be fabricated using readily available silicon processing (30-50μm).

RCE resonance may completely trap the photons in the resonant cavity and result in near-unity absorption efficiency. Farhoomand and McMurray suggested that the quantum efficiency in photodiodes with RCE processing may reach 100%, but at the cost of narrower spectral sensitivity [7]. Designs covering a wider spectral range were demonstrated by tuning adjacent pixels to different wavelengths while preserving high quantum efficiency. As long-range optical communications use narrow bandwidth lasers, narrow spectral sensitivity is actually a bonus for the detection system as it may partially filter out the optical background.

The quantum efficiency *QE* of p-n junction photodiodes is the product of the quantum absorption efficiency *QAE* (*QAE* = number of photo generated e-h pairs/number of incident photons) and the collection efficiency *CCE* of the photo-generated carriers across the p-n junction.

$$QE = QAExCCE \qquad (1)$$

Silicon GPD pixels in GPD arrays have low quantum efficiency (few percent) at λ=1064 nm due to weak absorption of the infrared photons (absorption depth is in the 1000 μm range [8]). Their quantum efficiency could be increased either by increasing the absorption thickness to hundreds of microns or by providing multiple photon paths in thin structures. The thick detector approach is not practical for arrays with small pixel size. Moreover, the need to deplete the absorption volume would require device operation at thousands of volts. Fortunately, RCE requires thin semiconductor layers (thin resonant cavities) and relatively low absorption losses in order for photodiodes to achieve close to 100% quantum absorption efficiency. As the diffusion length of the free carriers becomes much larger than the cavity thickness and the tail of the electric field may extend through the whole cavity, *CCE* may approach unity and the only limiting factor in achieving high quantum efficiency for the GPD structure design is the quantum absorption efficiency *QAE*. Therefore, in order to achieve high detection efficiency, we will investigate methods to enhance the quantum absorption efficiency

The generally accepted equation governing the detection efficiency DE in Geiger detectors is:

$$DE = 1 - \exp(-QE * n_{photons} * P_{be}) \tag{2}$$

where $n_{photons}$ is the number of photons/pulse, QE is the quantum efficiency and P_{be} is the single-carrier pair breakdown probability. Therefore, enhancements of single-photon detection efficiency require new detectors capable of increasing both the quantum efficiency and single carrier breakdown probability.

1.1 Short presentation of the resonant cavity concept

An extensive review and analysis of RCE detectors has been published elsewhere [9] - we will present here an abbreviated analytical formulation of the RCE effect needed to support the process development arguments and point to the technological challenges and improvements required to yield a robust RC-GPD array technology. Figure 1a shows the schematic of the RC-GPD structure. In practice, a thin GPD is placed between two distributed Bragg reflectors (mirrors) DBR1 and DBR2. *QAE* is a function of αd; the product between the absorption coefficient α and the GPD thickness d and is a periodic function of the NIR wavelength λ:

$$QAE = f(\alpha d, \cos(\lambda), R_1, R_2) \tag{3}$$

where R_1 and R_2 is the reflectance of the two DBR mirrors. The effect of the *QAE* enhancement at resonance is shown in Figure 1b. The rightmost plateau corresponds to the classical case of single-path, thick-base optical detectors. Because the photon path is enhanced through multiple trips inside the cavity, at resonance *QAE* may reach 100% even for detectors with thinner cavities. This should allow designing thin RC detector arrays with improved spatial resolution.

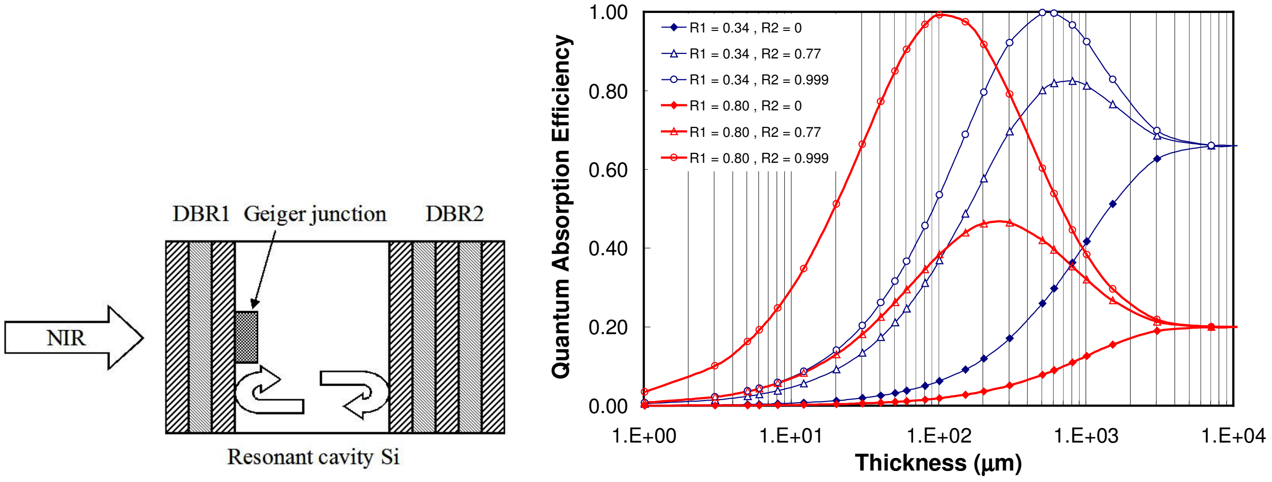

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Figure 1. (a) RC-GPD schematic structure. NIR photons pass through the distributed Bragg reflector DBR1 and generate electron-hole pairs in the silicon resonant cavity, the base of the GPD. Electron-hole pairs are multiplied through the Geiger process. At the resonant wavelength, NIR photons are multiply reflected by DBR1 and DBR2 thus increasing the quantum absorption efficiency in silicon.; (b) Calculated *QAE* in silicon at 1064nm for two sets of reflectance

mirrors shows that it is possible to design RCE structures with thinner base and achieve *QAE* ≈100%. NOTE: R_1 is the reflectance at mirror DBR1 and R_2 is the reflectance at mirror DBR2.

2. ANALYSIS OF RC-GPD DESIGN PARAMETERS

2.1 Analysis of the process parameters controlling *QAE*

Equation (3) indicates the cavity thickness *d* as the main process geometrical parameter controlling the resonance. We simulate the dependence of *QAE* on cavity thickness and cavity thickness uniformity. Surface roughness is treated as short-range cavity thickness non-uniformity.

QAE versus cavity thickness – optimal cavity thickness range

QAE was simulated for two cavities tuned to 1064nm - 34 µm and 64 um. The first cavity thickness is selected in the range for which we expect close to 100% carrier collection efficiency in our current GPD design. DBR1 and DBR2 are selected to yield near-optimal *QAE*. The simulation results are shown in Figure 2a and Figure 2b.

The simulation yields the following conclusions: (1) Thicker cavities are beneficial for *QAE* enhancement: and (2) The spacing of the cavity modes, (i.e., resonant wavelengths) defined as the free spectral range (FSR) as well as the resonant peak full-width at half-maximum (FWHM) decrease for thinner cavities. These results indicate that thicker cavities will yield higher *QAE* but at the expense of narrower peak width and consequently may result in more difficult control of the cavity thickness and may require increased laser center wavelength stability when integrated into the DSOC system. The selection of the optimal thickness will compound *QAE* and *CCE* criteria for a particular GPD structure. If GPD arrays are intended to be operated with integrated signal processing and readout electronics, today's CMOS readout logic requires low operation voltage GPD arrays and limited space charge extension. As our GPD arrays operate in the 13-14V range and the collection efficiency is high up to 30 µm GPD base (cavity) thickness, the *QAE* for thin RC-GPD array designs should be in the 40-60% range.

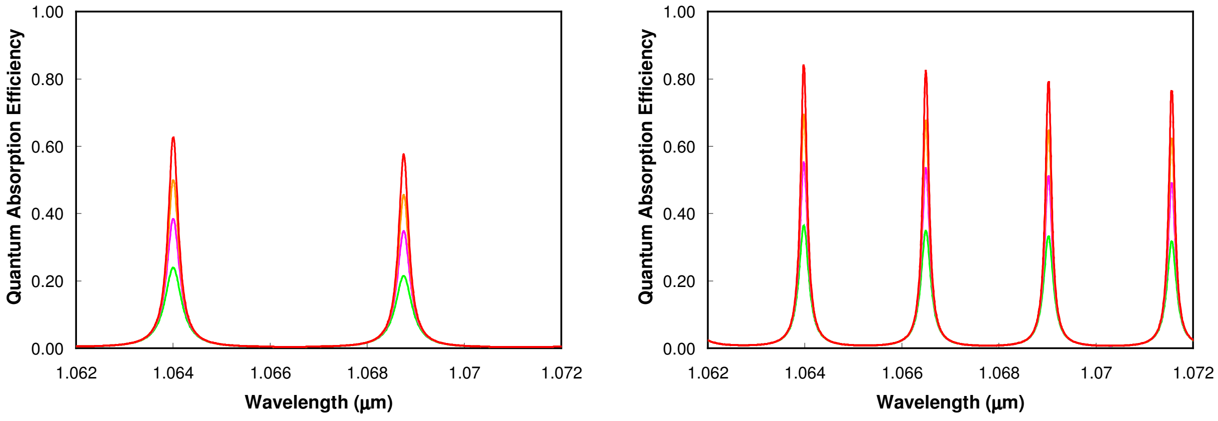

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Figure 2. Calculated *QAE* versus wavelength for two cavities tuned to yield resonance at 1064nm (34µm and 64µm) for four DBR1-DBR2 mirror sets.

Tuning to center wavelength

In order to assess the requirement of controlling the average cavity thickness, *QAE* was simulated for the optimal thickness (tuned at 1064nm) and two cavities 2nm off the thickness target. As shown in Figure 3, *QAE* is still greater than 50% even for a thickness excursion of 4nm.

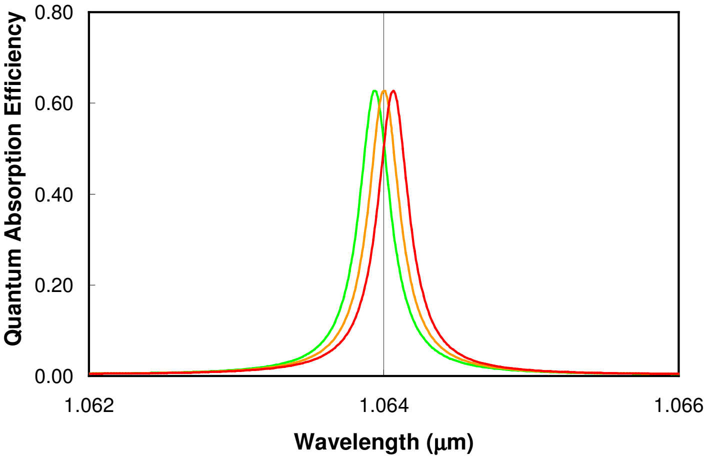

Figure 3. Simulated QAE for tuned cavity at 1064nm and two cavities 2nm off the target.

QAE versus surface roughness

Surface roughness scatters the resonant photons and thus decreases *QAE*. Epitaxial layer silicon is used for RC-GPD fabrication. Epitaxial layer roughness specifications range from 0.15nm sigma to 0.7nm. We identify the surface roughness, which could be treated as short-range cavity thickness non-uniformity as the second important cavity resonance control processing parameter. We evaluate in this section the *QAE* tolerance to surface roughness up to one order of magnitude higher than the specifications currently supported by wafer vendors (8nm). We plot the wavelength dependence of the *QAE* as a function of cavity thickness variation. As shown in Figure 4, a thickness variation in the order of several nanometers would be tolerable without significant loss in the peak efficiency. Even for an 8nm variation across the detector, a peak efficiency of 40% is achievable. While few-nm flatness can be easily achieved in Si device manufacturing over relatively short distance, fabricating large RC-GPD arrays may require backend correction procedures to compensate for long-range thickness non uniformity. Some variation of the cavity thickness across a device structure is tolerable - in fact, a modest thickness variation helps relaxing the peak laser wavelength stability by broadening the resonance.

DBR mirror selection

A RC-GPD cavity having fixed front side reflectance and with backside mirror reflectance R_2 ranging from 80% to 99% is shown in Figure 5. The performance increases monotonically over the selected range – the results show the benefit of processing high reflectance mirrors on the backside of the RC-GPD. Such mirror depositions processes are readily available from companies specializing in optical interferential filters and the cost/array in batch processing adds only 1-5% to the total processing cost.

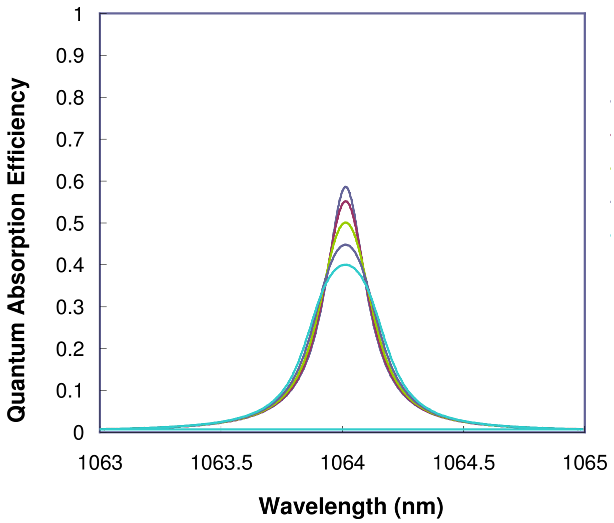

Figure 4. Simulation of the *QAE* for a nominal 34 µm cavity thickness and roughness ranging from 0nm to 8nm in 2nm increments. *QAE* decreases from 60% to 40% if the roughness is as high as 8nm.

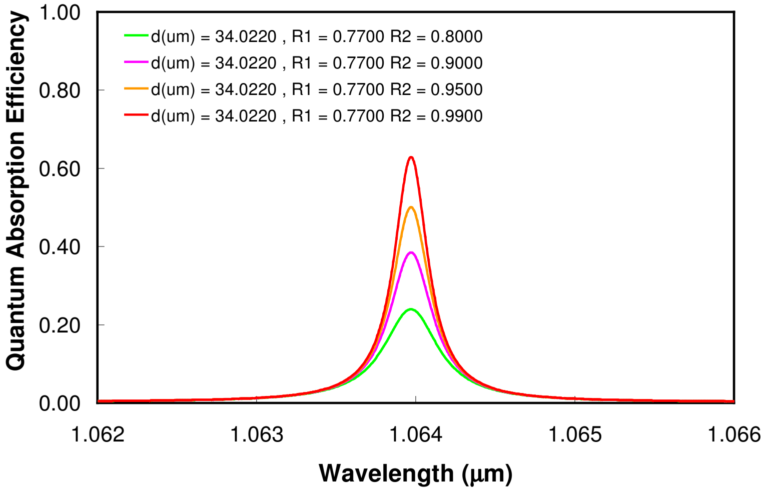

Figure 5. Simulated *QAE* for backside mirrors with reflectance ranging from 80% to 99%. *QAE*=65% for R_2=99%.

3. PERFORMANCE EVALUATION OF THE BACKEND PROCESS FLOW STEPS

3.1 Cavity thickness control

GPD array die, previously fabricated in standard CMOS, have been assembled in flip-chip technology on thermal expansion coefficient-matching handle substrates, then thinned to approximately 50 um and polished to 30um. The handle substrate, solder bump assembly and passivating layers have been optimized for minimal stress in the cavity membrane (extension 2000um x 2000um). Procedures to avoid cupping /rounding at the die edge have been identified, partially implemented and a plan for further optimization has been developed. Interferometry profiling of the whole die (Figure 6a) has shown an average surface flatness of 60 nm. Short range profiling on a region of interest, comparable with the pixel pitch (100um), has yielded less than 0.5nm roughness (best result is shown in Figure 6b, typical roughness hovers around 2-3nm). As expected, the tensile stress created by the dielectric/metal layers processed on the front surface has induced a bow up of the cavity membrane in the 50nm range over the device area (approximately 800µmx800µm). This membrane cavity deformation is not of concern, as the tilt angle should not noticeably degrade *QAE* performance. While the above results are an excellent proof of concept demonstration, achieving the tuning performance over the whole array area is challenging and requires developing *in-process* controls and sort procedures. Based on this process evaluation, we are currently developing mapping procedures combined with local cavity thickness processing to tune large arrays of RC-GPDs.

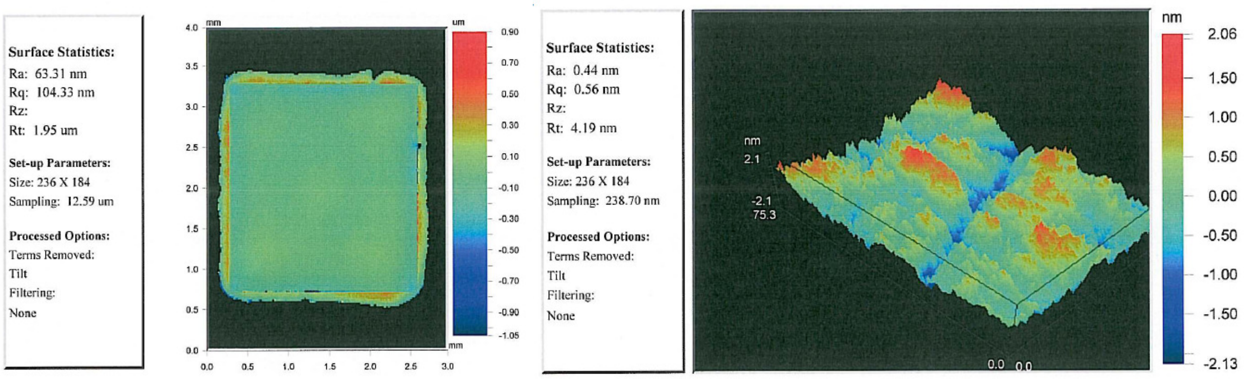

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Figure 6. Surface profiles after die thinning and polishing; (a) Overall RC-GPD array die surface profile; (b) Small area (50um x 75um), comparable with the GPD pixel pitch, shows less than 0.5nm roughness.

3.2 Back mirror fabrication stress evaluation

A process to fabricate the multi-layer DBR stack on the backside of the RC-GPD array, compatible with the low temperature requirements of the flip-chip assembly, has been successfully implemented. The mirror reflectance was selected to be only 94% at 1064nm with the goal to allow the injection of infrared photons from either the front side or the backside of the RC-GPD. The cavity profiling after DBR fabrication has shown minor increase of the back surface bow (from 50nm to 75 nm) in the GPD array device area.

4. RESULTS

4.1 Response to NIR photons

First generation thin cavity RC-GPDs with DBR2 reflecting 99.8% of the photon flux has shown about 10X increase of the photocurrent at 1050nm in backside illumination configuration as compared with standard thick base (about 300um) GPDs. A second generation RC-GPD array with integrated DBR2 mirror reflecting 94% is shown in Figure 7a (backside view). Its assembly has been modified to allow front side and backside illumination. A window was laser cut in the package to allow illumination from the front side (Figure 7b) with the goal to compare the relative detection efficiency performance in front illuminated and backside-illuminated modes.

These RC-GPD arrays have been tested at 1050nm in collimated beams. Comparative front-side versus backside photo current response measurements indicate significant lateral collection of the photo-generated carriers – the current ratio backside/frontside is about 30:1. If we assume the same collection efficiency for front or backside photo-generation, then the equivalent lateral collection area diameter on the backside is greater than 70µm. The detection efficiency (backside/frontside) ratio in Geiger mode at 1050 nm is only 1:6 indicating that, for the current GPD layout and junction structure, the front side detection is the configuration of choice for NIR detection. This large unbalance in the detection efficiency is expected as the Geiger avalanche multiplies only the electrical carriers generated in volume – laterally collected carriers pass through the low electric field at the Geiger junction periphery and are not multiplied [10]. No calibrated measurements of the detection efficiency have been performed, as the contribution of the laterally collected photocurrent would underestimate the detection efficiency – new self aligned test structures are planed to be implemented into the next RC-GPD layout design to allow extracting the contribution of the photocurrent passing through the Geiger junction only.


a

b

Figure 7. a) RC-GPD array backside view; (b) RC-GPD array front-side aperture view.

4.2 Timing jitter at 1050nm

A collimated 1050nm laser, emitting 35ps pulses, has been used for timing measurements. GPD pixels actively quenched by off-chip ASICs have been tested for timing jitter (rise time fluctuations or RTF) in multi-photon and single-photon regimes. The intrinsic RTF (corrected for measurement system RTF, ASIC RTF, and laser pulse width) was 150ps for single-photon registered photon hits and 20ps for multi-photon hits (Figure 8). No direct RTF performance evaluation has been attempted on RC-GPDs, as the parasitic capacitance in the current package assembly may degrade the timing performance of the Geiger pulse leading edge. A simplified estimate of the contribution of 1050nm photon multiple reflections in the resonant cavity of RC-GPD to RTF is provided instead. Indeed, if the absorption depth at 1050nm is 1000um, because after a trip of 2500um in the resonant cavity 90% of photons are absorbed, the collection of carriers due to delayed photon generation may increase RTF by 3.4*2500/c=28ps.

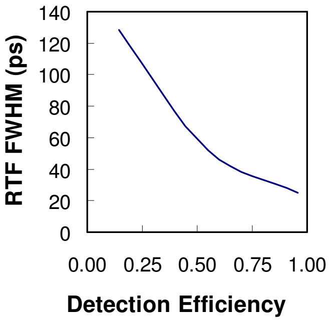

Figure 8. Measured RTF versus the GPD detection efficiency at 1050nm.

5. CONCLUSIONS

The quantification of the dependence of the quantum absorption efficiency on cavity processing parameters and the process steps development have shown that it is feasible to fabricate arrays of GPDs in a resonant cavity, tuned to NIR wavelengths. Moreover, the results indicate that the Geiger avalanche is capable of suppressing the lateral collection of photo generated carriers and thus allows designing higher spatial resolution photon-counting arrays. Technological challenges are related to how well the thickness could be controlled over large arrays to yield acceptable variability of the quantum efficiency performance. Current silicon processing technology is capable of meeting short-range thickness uniformity and surface roughness requirements. However tuning the cavity over large areas will require developing in-process procedures to control and tune locally the cavity. This evaluation phase has demonstrated that it is feasible to implement resonant cavity fabrication steps at the backend of the GPD array fabrication flow, thus preserving the advantage of using high-volume CMOS foundries to process RC-GPD arrays.

6. ACKNOWLEDGEMENT

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[10] In fact good GPD designs aim at creating very low electric fields on the junction periphery (as compared to the Geiger junction), thus protecting the Geiger junction from premature breakdown and allowing significant overbias above the breakdown voltage.
